Title:	Set Theoretic Processor Synthesis, Decomposition and Representation
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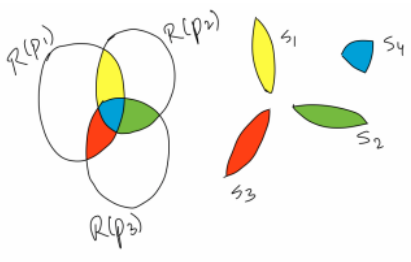
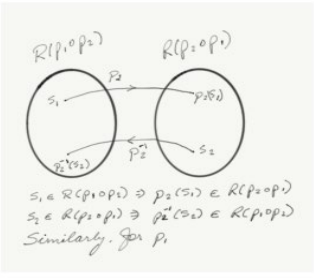
Keyword(s):	Subinclusion, Processor Composition, Preservance, Sub-uniform Rank
Subject(s):	Signals and Systems Permutation and Combination Set Theory
Abstract:	Fundamental research is imperative to innovation. It serves to take the frontiers of knowledge a step further in a given area. A definite theoretical model provides a powerful backing to any complex idea and the confidence of its realisation in initial attempts. This thesis aims to serve such a function in the field of signals and systems. It develops on a purely set-theoretic built theory of signals and systems. The attraction of the set theoretic formulation lies in its generality. The fewer assumptions a theory makes, the more widely applicable it becomes. Therefore, this theory is not confined to the dimensions of signals and systems but can rather be used in any field using permutation. In this context, this thesis provides a representation of the processor space and examines the question of the degree to which a processor space can be analysed based on its preservance sequence. An in-depth theoretical study of the processor space is illustrated to understand the representation. The question of the analysis degree is addressed employing the properties of sub inclusion and preservance. The representation of the processor space facilitate in providing a basis of the complete space reducing its order (in terms of number of signals in the signal space) from exponential to linear. The results deduced in this study can be employed to reduce the complexity of any problem which can be solved through the study of a processor's composition parts. Also highlighted is the non-uniqueness of this decomposition. The analysis of the processor space based on the preservance sequence proves useful in depicting a much finer relationship between any two given processors than is provided based on synthesizability. This study also presents a method that eliminates the need to mechanically evaluate the (generally indefinite) complete preservance sequence to evaluate this relationship and determine if two given processors have the same preservance sequence. Future directions are suggested to relate a processor's preservance sequence characteristics to the preservance sequence characteristics of the basis processors it can be decomposed into.





Domain	p	p'
s_1	s_3	s_3
s_2	s_1	s_1
s_3	s_2	s_2
s_4	s_1	s_3

Table 1.6: Processors with same $R^{[1]}$

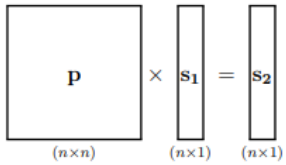


Figure 2.1: Processor Matrix

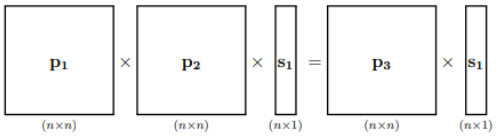


Figure 2.3: Processor Matrix Multiplication

Domain	p_1
s_1	s_2
s_2	s_4
s_3	s_5
s_4	s_1
s_5	s_6
s_6	s_3

Table 2.2: Example Processor

Domain	p_1	p_2
s_1	s_1	s_6
s_2	s_2	s_2
s_3	s_4	s_3
s_4	s_3	s_4
s_5	s_5	s_5
s_6	s_6	s_1

Table 2.4: Example Dijoint Set SBP

Domain	p_1
s_1	s_1
s_2	s_2
s_3	s_4
s_4	s_3
s_5	s_5
s_6	s_6

Table 2.3: Example SBP